



Europäisches Patentamt  
European Patent Office  
Office européen des brevets



Publication number: 0 428 330 A3

BS

# EUROPEAN PATENT APPLICATION

Application number: 90312210.9

Int. Cl.<sup>5</sup>: G06F 13/30, G06F 13/32

Date of filing: 08.11.90

Priority: 13.11.89 US 434385

Date of publication of application:  
22.05.91 Bulletin 91/21

Designated Contracting States:  
BE CH DE FR GB IT LI NL SE

Date of deferred publication of the search report:  
04.11.92 Bulletin 92/45

Applicant: International Business Machines Corporation  
Old Orchard Road  
Armonk, N.Y. 10504(US)

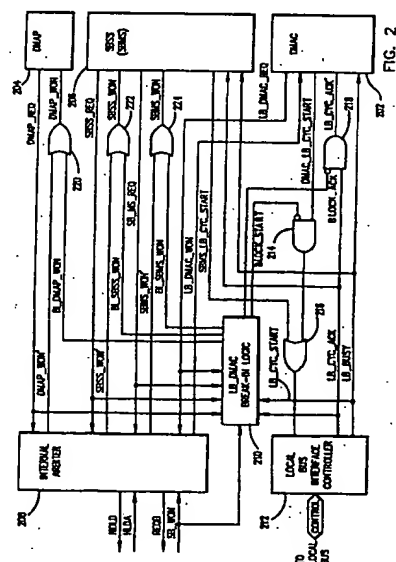
Inventor: Garcia, Serafin Jose Eleazer, Jr.  
304 Buttonwood Lane

Boynton Beach, Florida 33436(US)  
Inventor: Chisholm, Douglas Roderick  
3512 Blvd.Chatelaine  
Delray Beach, Florida 33445(US)  
Inventor: Kalman, Dean Alan  
1402 Copley Court  
Lantana, Florida 33462(US)  
Inventor: Padgett, Russell Stephen  
51 Sparrow Drive  
Royal Palm Beach, Florida 33411(US)  
Inventor: Yoder, Robert Dean  
5189 Jog Lane  
Delray Beach, Florida 33484(US)

Representative: Burt, Roger James, Dr.  
IBM United Kingdom Limited Intellectual  
Property Department Hursley Park  
Winchester Hampshire SO21 2JN(GB)

Computer Interface circuit.

A plurality of specialized controllers, e.g. 202, 204 & 206, each one adapted to control a particular type of data transfer operation, control the flow of data between a system bus 104 and a local bus 106 on a computer adapter card 102. When the Direct Memory Access DMA controller 202 is controlling a DMA operation on the local bus, certain other controllers 204 & 206 can break-in to the current DMA operation, temporarily halting the DMA operation until the other controller has completed its data transfer operation. To break-in to a DMA operation, handshaking signals between the DMA controller and the local bus interface circuit 212 are temporarily blocked by blocking signals from a break-in logic circuit 210. The break-in circuit includes a four-state state machine to block the handshaking signals at the appropriate times, and to signal the interrupting controller to begin its data transfer operation. When breaking-in to a DMA operation in this manner, the operation of the DMA controller is not altered; instead, to the DMA controller, it appears that the local bus interface circuit is merely slow to respond with its acknowledge handshake.



BEST AVAILABLE COPY